IN THE CLAIMS

Please amend the claims as follows:

1. (original) A VLIW processor comprising

a plurality of functional units, each for executing an operation, and a VLIW controller connected to each of said functional units and adapted to control said functional units characterized by

at least one indication means associated with one of said functional units and adapted to register and indicate to the VLIW controller whether said one functional unit is idle or operating.

2. (original) The VLIW processor of claim 1,

wherein said indication means is adapted to register whether said one functional unit receives data for executing its operation and whether said one functional unit outputs data after executing its operation.

3. (original) The VLIW processor of claim 2,

wherein said indication means comprises an input register for inputting data to said one functional unit and an output register for receiving data output from said one functional unit, said input

and output register each comprising a presence bit indicative of the presence or absence of data in the respective register.

4. (original) The VLIW processor of claim 3, wherein said input register is adapted to trigger the execution of the operation by said one functional unit, if data is present in the input register.

5. (original) The VLIW processor of claim 3, wherein said indication means comprises an input register file having a plurality of said input registers and an output register file having a plurality of said output registers.

6. (original) The VLIW processor of claim 5, wherein the input register file is adapted to trigger the execution of the operation by said one functional unit, if a predetermined number of the input registers contain data.

7. (currently amended) The VLIW processor of claim 2~~ or 3~~, comprising a temporary register for storing data to be used repeatedly by said one functional unit, said temporary register being connected to said one functional unit.

8. (original) The VLIW processor of claim 5,
wherein the output register file is adapted to trigger the execution of the operation of a second functional unit, if a predetermined number of output registers contain data.

9. (currently amended) The VLIW processor of ~~one of the preceding claims~~claim 1,
wherein said one functional unit has a variable long latency.

10. (currently amended) The VLIW processor of ~~one of the preceding claims~~claim 1,
wherein the latency of the one functional unit depends on the data to be processed by said functional unit.

11. (original) Method of processing data in a VLIW processor, comprising the steps:
registering whether a functional unit is idle or operating; and
indicating to said VLIW controller whether said functional unit is idle or operating.

12. (original) The method of claim 11,
wherein said registering step comprises the steps

registering whether said one functional unit receives data for executing its operation and whether said one functional unit outputs data after executing its operation.

13. (original) The method of claim 12,
comprising the steps of
indicating to the VLIW controller that the functional unit receives data, and
indicating to the VLIW controller that the functional unit outputs data.